claims as newly renumbered by Examiner.

LISTING OF CLAIMS:

The following listing of claims replaces all previous versions, or listings, of claims in the present application.

Please cancel claims 40-42.

1. (Previously presented) A semiconductor device comprising:

a semiconductor substrate;

a plurality of cell blocks provided on the semiconductor substrate, wherein each cell block includes a plurality of transistor cells;

a plurality of gate electrodes formed in each of the plurality of cell blocks, wherein the plurality of gate electrodes of one cell block are electrically independent of the plurality of gate electrodes of other cell blocks; and

a plurality of gate pads provided on the semiconductor substrate corresponding to the plurality of cell blocks, wherein each of the plurality of gate pads is connected to one of the plurality of gate electrodes of the corresponding cell block.

2. (Previously presented) The semiconductor device according to claim 1, wherein:

the semiconductor substrate has a rectangular shape; and

the plurality of gate pads are arranged along a side of the semiconductor substrate.

3. (Previously presented) The semiconductor device according to claim 1, further comprising:

a ground terminal provided outside of the semiconductor substrate; and

a gate terminal provided outside of the semiconductor substrate, the gate terminal being electrically independent of the ground terminal, wherein:

the plurality of cell blocks includes a first non-defective cell block and a second defective cell block; and

the plurality of gate pads includes a first gate pad that connects the first non-defective cell block to the gate terminal, and a second gate pad that connects the second defective cell block to the ground terminal.

4. (Previously presented) The semiconductor device according to claim 3, wherein:

the first gate pad is bonded to the gate terminal by one of wire-bonding, soldering, and pressure-welding; and

the second gate pad is bonded to the ground terminal by one of wire-bonding, soldering, and pressure-welding.

5. (Previously presented) The semiconductor device according to claim 1, further comprising:

a gate terminal provided outside of the semiconductor substrate;

a source or emitter pad provided on the semiconductor substrate, wherein the source or emitter pad has a source potential or an emitter potential, wherein:

the plurality of cell blocks includes a first non-defective cell block and a second defective cell block; and

the plurality of gate pads includes a first gate pad that connects the first non-defective cell block to the gate terminal, and a second gate pad that connects the second defective cell block to the emitter or source pad.

6. (Previously presented) The semiconductor device according to claim 5, wherein:

the first gate pad is bonded to the gate terminal by one of wire-bonding, soldering, and pressure-welding; and

the second gate pad is bonded to the source or emitter pad by one of wire-bonding, soldering, and pressure-welding.

7. (Previously presented) The semiconductor device according to claim 1, wherein the semiconductor substrate is an insulated gate type bipolar transistor chip.

8. (Previously presented) The semiconductor device according to claim 1, further comprising a plurality of marks provided at a plurality of regions of the semiconductor substrate, wherein the plurality of marks respectively corresponds to the plurality of cell blocks, each of the plurality of marks being for discriminating whether a corresponding cell block is defective.

9. (Previously presented) The semiconductor device according to claim 8, wherein discrimination of whether each of the plurality of cell blocks is defective is determined by at least one of location, color, size, and shape of a corresponding one of the plurality of marks.

10. (Previously presented) The semiconductor device according to claim 8, wherein discrimination of whether each of the plurality of cell blocks is defective is determined by a number of the plurality of marks corresponding to each of the plurality of cell blocks.

11. (Previously presented) The semiconductor device according to claim 8, wherein:

the plurality of cell blocks includes a first cell block;

the plurality of gate pads includes a first gate pad connected with the first cell block; and

the plurality of marks includes a first mark for discriminating whether the first cell block is defective, the first mark being provided on a line passing through the first gate pad.

12. (Previously presented) The semiconductor device according to claim 11, wherein the first mark is provided at a side of the first gate pad opposite to the first cell block.

13. (Previously presented) The semiconductor device according to claim 11, wherein:

the plurality of cell blocks includes a second cell block;

the plurality of gate pads includes a second gate pad connected with the second cell block;

the plurality of marks includes a second mark for discriminating whether the second cell block is defective, the second mark being located apart from a line passing through a center of the second gate pad.

14. (Previously presented) The semiconductor device according to claim 8, wherein each of the plurality of marks is located in a vicinity of a corresponding gate pad or on a surface of the corresponding gate pad.

15 (Previously presented) The semiconductor device according to claim 8, wherein the plurality of marks can be recognized by an image recognition device of a wire-bonding apparatus.

16. (Previously presented) The semiconductor device according to claim 1, further comprising a plurality of pads having an emitter potential and provided on the semiconductor substrate adjacent to the plurality of gate pads.

17. (Previously presented) The semiconductor device according to claim 16, further comprising a gate terminal provided outside of the semiconductor substrate, wherein:

the plurality of cell blocks includes a first cell block and a second cell block, the first cell block being non-defective and connected with the gate terminal and the second cell block being defective and connected with one of the plurality of pads having an emitter potential.

18. (Previously presented) The semiconductor device according to claim 17, further comprising:

a plurality of emitter electrodes respectively provided in the plurality of cell blocks;

a plurality of emitter pads provided on a main surface of the semiconductor substrate and respectively connected with the plurality of emitter electrodes;

a collector electrode provided on a back surface of the semiconductor substrate;

an emitter terminal bonded to the main surface of the semiconductor substrate and electrically connected with the plurality of emitter pads;

a collector terminal bonded to the back surface of the semiconductor substrate and electrically connected with the collector electrode; and

a resin member encapsulating the gate terminal, the emitter terminal, and the collector terminal together.

19. (Previously presented) The semiconductor device according to claim 17, further comprising:

a plurality of emitter electrodes respectively provided in the plurality of cell blocks;

a plurality of emitter pads provided on a main surface of the semiconductor substrate and respectively connected with the plurality of emitter electrodes; and

an emitter terminal provided outside of the semiconductor substrate and electrically connected with the emitter pads, wherein:

the first cell block is connected to the gate pad through a first bonding wire; and

the second cell block is connected to the one of the plurality of pads through a second bonding wire.

20. (Previously presented) The semiconductor device according to claim 16, further comprising a gate terminal provided outside of the semiconductor device, wherein:

the plurality of cell blocks includes a first group of cell blocks, which have an equal threshold voltage and are connected with the gate terminal, and a second group of cell blocks, which have different threshold voltages from one another and are connected with one of the plurality of pads.

21-37 (Canceled)

38. (Previously presented) An apparatus for manufacturing an insulated gate type power IC, comprising:

a chip transfer machine including a plurality of trays for selectively holding a plurality of chips, wherein each chip includes:

a semiconductor substrate;

a plurality of cell blocks on the substrate, wherein each cell block includes a plurality of transistor cells;

a plurality of gate electrodes formed in each of the plurality of cell blocks, wherein the plurality of gate electrodes of one cell block is electrically independent of the plurality of gate electrodes of others of the plurality of cell blocks; and

a plurality of gate pads on the substrate and respectively corresponding to the plurality of cell blocks, wherein each gate pad is connected to the plurality of gate electrodes of a corresponding cell block; wherein:

the plurality of chips is sorted based on an arrangement position of a defective cell block of each chip in one of the plurality of trays;

the defective cell block has a corresponding gate pad that is connected with one of a ground terminal having a ground potential and an emitter pad having an emitter potential; and

a non-defective cell block of each of the plurality of chips has a corresponding gate pad that is connected with a gate terminal provided outside of the semiconductor substrate.

39. (Previously presented) An insulated gate type power IC module that includes a plurality of insulated gate type ICs, each of the insulated gate type ICs comprising:

a semiconductor substrate;

a plurality of cell blocks located on the substrate each of which includes a plurality of transistor cells;

a plurality of gate electrodes formed in each of the cell blocks, wherein the plurality of gate electrodes of one cell block is electrically independent of the plurality of gate electrodes of others of the plurality of cell blocks; and

a plurality of gate pads on the substrate corresponding to the plurality of cell blocks, wherein each of the plurality of gate pads is connected to the plurality of gate electrodes of a corresponding cell block; wherein:

each of the insulated gate type ICs includes a defective cell block at an identical position and a non-defective cell block, the defective cell block having a corresponding gate electrode that is connected with one of a ground terminal provided outside of the semiconductor substrate and an emitter pad provided on the semiconductor substrate, the non-defective cell block having a corresponding gate electrode that is connected with a gate terminal provided outside of the semiconductor substrate; and

the insulated gate type power IC module is composed exclusively of the plurality of insulated gate type ICs.

40-42. (Canceled)

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43. (Currently amended) ~~The semiconductor device according to claim 41, further comprising~~ A semiconductor device comprising:

a plurality of transistor cells arranged in a semiconductor chip and divided equally into a plurality of groups, wherein each of the plurality of transistor cells comprises a source electrode on a surface side of the semiconductor chip and a drain electrode on a back side of the semiconductor chip;

a plurality of common gate electrodes for the plurality of groups, respectively;

a plurality of gate pads for the plurality of common gate electrodes, respectively, wherein each of the plurality of gate pads is located on the surface side of the semiconductor chip;

a gate terminal bonded to certain of the plurality of gate pads with wires;

a source terminal commonly soldered to the source electrode; and

a drain terminal commonly soldered to the drain electrode.

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44. (Previously presented) The semiconductor device according to claim 43, further comprising a coating of resin encapsulating the semiconductor chip, the wires, part of the gate terminal, and part of the drain terminal.

25 45. (Currently amended) ~~The semiconductor device according to claim 42, further comprising:~~ A semiconductor device comprising:

a plurality of transistor cells arranged in a semiconductor chip and divided equally into a plurality of groups, wherein each of the plurality of transistor cells comprises a source electrode on a surface side of the semiconductor chip and a drain electrode on a back side of the semiconductor chip;

a plurality of common gate electrodes for the plurality of groups, respectively;

a plurality of gate pads for the plurality of common gate electrodes, respectively, wherein each of the plurality of gate pads is located on the surface side of the semiconductor chip;

an equipotential pad adjacent to the plurality of gate pads, wherein a source potential is applied to the equipotential pad;

a gate terminal bonded to certain of the plurality of gate pads with wires;

a source terminal commonly soldered to the source electrode; and

a drain terminal commonly soldered to the drain electrode.

26 46. (Previously presented) The semiconductor device according to claim 45, wherein the equipotential pad is provided for a gate pad corresponding to one of the plurality of groups including a possibly defective transistor cell to be bonded with a wire.

27 47. (Previously presented) The semiconductor device according to claim 46, further comprising a coating of resin encapsulating the semiconductor chip, the wires, part of the gate terminal, and part of the drain terminal.

28 48. (Currently amended) ~~The semiconductor device according to claim 42~~A semiconductor device comprising:

a plurality of transistor cells arranged in a semiconductor chip and divided equally into a plurality of groups, wherein each of the plurality of transistor cells comprises a source electrode on a surface side of the semiconductor chip and a drain electrode on a back side of the semiconductor chip;

a plurality of common gate electrodes for the plurality of groups, respectively;

a plurality of gate pads for the plurality of common gate electrodes, respectively, wherein each of the plurality of gate pads is located on the surface side of the semiconductor chip;

wherein the semiconductor device further comprises an equipotential pad adjacent to the plurality of gate pads, wherein a source potential is applied to the equipotential pad, and the equipotential pad is provided for one of the plurality of gate pads corresponding to one of the plurality of groups including a possibly defective transistor cell to be bonded with a wire.

29 49. (Currently amended) ~~The semiconductor device according to claim 40, further comprising~~ A semiconductor device comprising:

a plurality of transistor cells arranged in a semiconductor chip and divided equally into a plurality of groups;

a plurality of common gate electrodes for the plurality of groups, respectively;

a plurality of gate pads for the plurality of common gate electrodes, respectively; and

means for preventing one of the plurality of groups that includes a possibly defective transistor cell from operating.

30 50. (Previously presented) The semiconductor device according to claim 49, wherein the preventing means includes means for applying a ground potential or a source potential to a corresponding common gate electrode through a corresponding gate pad.

51. (Currently amended) The semiconductor device according to claim ~~41~~43, wherein the plurality of transistor cells forms an insulated gate bipolar transistor in which the source electrode serves as an emitter and the drain electrode serves as a collector.

52. (New) The semiconductor device according to claim ~~45~~, wherein the plurality of transistor cells forms an insulated gate bipolar transistor in which the source electrode serves as an emitter and the drain electrode serves as a collector.

53. (New) The semiconductor device according to claim ~~48~~, wherein the plurality of transistor cells forms an insulated gate bipolar transistor in which the source electrode serves as an emitter and the drain electrode serves as a collector.

54. (New) The semiconductor according to claim ~~49~~ wherein:

each of the plurality of transistor cells comprises a source electrode on a surface side of the semiconductor chip and a drain electrode on a back side of the semiconductor chip, wherein each of the plurality of gate pads is located on the surface side of the semiconductor chip; and

the plurality of transistor cells forms an insulated gate bipolar transistor in which the source electrode serves as an emitter and the drain electrode serves as a collector.